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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,892	01/21/2004	Tien-Jen Cheng	FIS920030352US1	1891

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INTERNATIONAL BUSINESS MACHINES CORPORATION
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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,892	CHENG ET AL.	
	Examiner	Art Unit	
	Matthew C. Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-14 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-14 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 27, 2007 has been entered.

Claim Objections

Claim 21 is objected to because of the following informalities: an extra comma exists in the fifth line of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 8 recites the limitation "said conducting layer pad". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (US PGPub 2005/0103636, hereinafter Cheng).

The applied reference has a common assignee/inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 5, and 7, Figure 6 of Cheng discloses a terminal metal layer 106/102 disposed on a passivating layer 108/110; a diffusion barrier layer (116 and the CrCu portion of 118) on said terminal metal layer; a conducting layer pad (Cu portion of 118) on said diffusion barrier; a hard test barrier layer (Ni) 122 (paragraph [0014]) on, and enclosing, said conducting layer pad, wherein said hard test barrier layer extends along the sides of said conducting layer pad and said conducting layer pad is completely enclosed by said diffusion barrier layer and said hard test barrier; and a plate passivating layer (Au) 124 (paragraph [0014]) on said hard test barrier. Note that Cheng discloses layer 118 can be a multi-layered structure of Cu/CrCu (paragraph [0013]). Therefore, the Cu layer is considered to be the conducting layer pad, and the CrCu layer is considered to be part of the diffusion layer.

Regarding claims 2-4 and 22-24, Figure 6 of Cheng discloses said diffusion barrier layer includes an adhesion layer (CrCu portion of 118) on barrier metallurgy (TiW) 116 (paragraph [0013]).

Regarding claims 21 and 25, Figure 6 of Cheng discloses a terminal metal layer 106/102 disposed on a passivating layer 108/110; a diffusion barrier layer (116 and the CrCu portion of 118) on said terminal metal layer; a copper seed layer pad (Cu portion of 118) on said diffusion barrier; a nickel layer 122 (paragraph [0014]) plated to, and enclosing, said copper seed layer pad, wherein said nickel layer extends along the sides of said copper seed layer pad and said copper seed layer pad is completely enclosed by said diffusion barrier layer and said nickel layer; and a plate passivating layer (Au) 124 (paragraph [0014]) on said nickel layer. Note that Cheng discloses layer 118 can be a multi-layered structure of Cu/CrCu (paragraph [0013]). Therefore, the Cu layer is considered to be the copper seed layer pad, and the CrCu layer is considered to be part of the diffusion layer.

Claims 1, 2, 5, 7, 21, 22, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Biggs et al. (US PGPub 2005/0062170, hereinafter Biggs).

The applied reference has a common assignee/inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived

from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 5, and 7, Figure 6 of Biggs discloses a terminal metal layer 16/18 disposed on a passivating layer 12/14; a diffusion barrier layer 36 on said terminal metal layer; a conducting layer pad 38 on said diffusion barrier; a hard test barrier layer (Ni) 48 (paragraph [0012]) on, and enclosing, said conducting layer pad, wherein said hard test barrier layer extends along the sides of said conducting layer pad and said conducting layer pad is completely enclosed by said diffusion barrier layer and said hard test barrier; and a plate passivating layer (Au) 50 (paragraph [0012]) on said hard test barrier.

Regarding claims 2 and 22, Biggs discloses layer 36 consists of a layer of Ta and a layer of TaN (paragraph [0008]). The Ta layer can be considered the adhesion layer and the TaN layer can be considered the barrier metallurgy.

Regarding claims 21 and 25, Figure 6 of Biggs discloses a terminal metal layer 16/18 disposed on a passivating layer 12/14; a diffusion barrier layer 36 on said terminal metal layer; a copper seed layer pad 38 on said diffusion barrier; a nickel layer 48 (paragraph [0012]) plated to, and enclosing, said copper seed layer pad, wherein said nickel layer extends along the sides of said copper seed layer pad and said copper seed layer pad is completely enclosed by said diffusion barrier layer and said nickel layer; and a plate passivating layer (Au) 50 (paragraph [0012]) on said nickel layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-13 are rejected under 35 U.S.C. 102(e) as anticipated by Cheng or, in the alternative, under 35 U.S.C. 103(a) as obvious over Cheng in view of McCormick (US Pat. 6,706,622).

Regarding claims 8 and 11-13, Figure 6 of Cheng discloses a durable chip pad comprising: a terminal metal layer 106/102 disposed on a passivating layer 108/110 and connecting to underlying chip wiring through a via through said passivating layer; an adhesion/barrier layer (116 and the CrCu portion of 118) on said terminal metal layer; a seed pad (Cu portion of 118) on said adhesion/barrier layer; a hard test barrier layer (Ni) 122 (paragraph [0014]) plated on, and enclosing, said seed pad, wherein said hard test barrier layer extends along the sides of said conducting layer pad and said conducting layer pad is completely enclosed by said diffusion barrier layer and said hard test barrier; and a plate passivating layer (Au) 124 (paragraph [0014]) on said hard test barrier. Note that Cheng discloses layer 118 can be a multi-layered structure of Cu/CrCu (paragraph [0013]). Therefore, the Cu layer is considered to be the conducting layer pad, and the CrCu layer is considered to be part of the diffusion layer. Cheng discloses the passivating layer is formed on a semiconductor substrate (paragraph [0007]). This substrate is considered to be the IC chip. Cheng does not specifically disclose more than one pad on the chip. However, it is inherent that more than one pad is formed on the chip, since a chip

with only one connection pad would be useless. Assuming, *arguendo*, Applicant can prove having more than one pad is not inherent; the claim would be obvious in view of McCormick. Figure 6 of McCormick discloses a plurality of interconnect pads formed on an IC chip. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Cheng by including more than one pad as taught by McCormick for the purpose of allowing separate electrical connections to different portions of the IC.

Regarding claims 9 and 10, Figure 6 of Cheng discloses said adhesion/barrier layer includes an adhesion layer (CrCu portion of 118) on barrier metallurgy (TiW) 116 (paragraph [0013]).

Claims 8 and 11-13 are rejected under 35 U.S.C. 102(e) as anticipated by Biggs or, in the alternative, under 35 U.S.C. 103(a) as obvious over Biggs in view of McCormick

Regarding claims 8 and 11-13, Figure 6 of Biggs discloses a durable chip pad on an IC chip 10, comprising: a terminal metal layer 16/18 disposed on a passivating layer 12/14 and connecting to underlying chip wiring through a via through said passivating layer; an adhesion/barrier layer 36 on said terminal metal layer; a copper seed pad 38 on said adhesion/barrier layer; a hard test barrier layer (Ni) 48 (paragraph [0012]) plated on, and enclosing, said seed pad, wherein said hard test barrier layer extends along the sides of said conducting layer pad and said conducting layer pad is completely enclosed by said diffusion barrier layer and said hard test barrier; and a plate passivating layer (Au) 50 (paragraph [0012]) on said hard test barrier. Biggs does not specifically disclose more than one pad on the chip.

However, it is inherent that more than one pad is formed on the chip, since a chip with only one connection pad would be useless. Assuming, *arguendo*, Applicant can prove having more than one pad is not inherent; the claim would be obvious in view of McCormick. Figure 6 of McCormick discloses a plurality of interconnect pads formed on an IC chip. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Biggs by including more than one pad as taught by McCormick for the purpose of allowing separate electrical connections to different portions of the IC.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (or Cheng in view of McCormick) as applied to claim 13 above, and further in view of Homma et al. (US Pat. 6,798,050, hereinafter Homma) and Bhattacharya et al. (US PGPub 2003/0034489, hereinafter Bhatt).

Regarding claim 14, semiconductor IC chips are fabricated from a wafer of semiconductor material, and the wafer is not diced into individual chips until after the ICs have been completed. Therefore, in order to make the device of Cheng, there must have been a plurality of IC chips on a wafer at an intermediate stage of processing. However, Cheng does not explicitly disclose that the wafer is diced into individual IC chips after forming the claimed metal layers on the IC chip substrate. Figures 9A-9E of Homma discloses forming a plurality of metal layers on a wafer prior to dicing the wafer into individual chips (col. 11, lines 38-41). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Cheng by dicing the wafer after forming

the claimed metal layers, thereby resulting in a plurality of ICs (with the claimed structure) on a wafer. The ordinary artisan would have been motivated to further modify Cheng in the manner described above for the purpose of simply the production process for mass production. A further difference between Cheng and the claimed invention is the ICs are identical. Bhatt discloses forming a plurality of identical ICs on a wafer (paragraph [0030]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Cheng by having a plurality of identical ICs on a wafer for the purpose of simplifying the production process for mass production of a particular IC. Note that paragraph [0003] of the instant application gives a special definition to the word "die" by stating, "Each array location is known as a die and each die may harbor an IC chip". In other words, a "die" is simply the portion of the wafer where the chip is located. Therefore, it is inherent that each of said plurality of identical ICs are located in a die on said wafer.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Biggs (or Biggs in view of McCormick) as applied to claim 13 above, and further in view of Homma and Bhatt.

Regarding claim 14, semiconductor IC chips are fabricated from a wafer of semiconductor material, and the wafer is not diced into individual chips until after the ICs have been completed. Therefore, in order to make the device of Biggs, there must have been a plurality of IC chips on a wafer at an intermediate stage of processing. However, Biggs does not explicitly disclose that the wafer is diced into individual IC chips after forming the claimed metal layers on the IC chip substrate. Figures 9A-9E of Homma discloses forming a plurality of metal

layers on a wafer prior to dicing the wafer into individual chips (col. 11, lines 38-41). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Biggs by dicing the wafer after forming the claimed metal layers, thereby resulting in a plurality of ICs (with the claimed structure) on a wafer. The ordinary artisan would have been motivated to further modify Biggs in the manner described above for the purpose of simply the production process for mass production. A further difference between Biggs and the claimed invention is the ICs are identical. Bhatt discloses forming a plurality of identical ICs on a wafer (paragraph [0030]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Biggs by having a plurality of identical ICs on a wafer for the purpose of simplifying the production process for mass production of a particular IC. Note that paragraph [0003] of the instant application gives a special definition to the word "die" by stating, "Each array location is known as a die and each die may harbor an IC chip". In other words, a "die" is simply the portion of the wafer where the chip is located. Therefore, it is inherent that each of said plurality of identical ICs are located in a die on said wafer.

Response to Arguments

Applicant's arguments filed April 27, 2007 have been fully considered but they are not persuasive.

Applicant argues that "Cheng et al. teaches the passivating layer 112 over the terminal metal layer 102" and that this structure is different from claim 1 which requires "a terminal metal

layer disposed on a passivating layer". However, the above rejection indicates that the claimed passivating layer reads on layers 108/110 shown in Figure 6 of Cheng. Terminal metal layer 102 is clearly on the lower 108/110 pair. There is no reason why dielectric layers 108/110 cannot be considered a passivating layer. Applicant further argues that Cheng et al. cannot be used in a 103 rejection because it is only available under 102(e) and is commonly assigned. However, 35 U.S.C. §103(c) (1) states:

"Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person."

The fact that the reference and the application have the same assignee is not, by itself, sufficient evidence to disqualify the prior art under 35 U.S.C. 103(c). There must be a statement that the common ownership was "at the time the invention was made." Applicant has not made this key statement. Furthermore, claims 8-13 were rejection under 102/103. Applicant has not responded to the 102(e) aspect of this rejection.

Applicant argues that, "Biggs et al. also teaches the passivating layer 30 over the terminal metal layer (aluminum pad 18)" and that this structure is different from claim 1 which requires "a terminal metal layer disposed on a passivating layer". However, the above rejection indicates that the claimed passivating layer reads on layers 12/14 shown in Figure 6 of Biggs. Terminal metal layer 16/18 clearly resides on the layer 12/14. There is no reason why dielectric layer 12/14 cannot be considered a passivating layer. Applicant further argues that Biggs et al. cannot be used in a 103 rejection because it is only available under 102(e) and is commonly assigned. However, 35 U.S.C. §103(c) (1) states:

"Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person."

The fact that the reference and the application have the same assignee is not, by itself, sufficient evidence to disqualify the prior art under 35 U.S.C. 103(c). There must be a statement that the common ownership was "at the time the invention was made." Applicant has not made this key statement. Furthermore, claims 8-13 were rejection under 102/103. Applicant has not responded to the 102(e) aspect of this rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is 571-272-1731. The examiner can normally be reached on 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew C. Landau
Primary Examiner
Art Unit 2815
8/3/07